

ITB test results Phase-1 ladder-1

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Introduction and test goals

The development of the PXL detector readout cable is a four step process described in [1]. The Infrastructure Testing Board (ITB) is the first step in the process and consists of running 10 sensors in a ladder configuration. The primary goal of this prototype is to assemble a functional and configurable ladder composed of 10 working sensors and then to find and test the working envelope of bypass capacitance and power supply and ground connections.

ITB - ladder 1 is composed of 9 full thickness (~700 μm) Phase-1 prototype sensors and one full thickness (~700 μm) Phase-2 prototype sensor, which is the second chip in the chain. The layout of the board is presented in Figure 1.

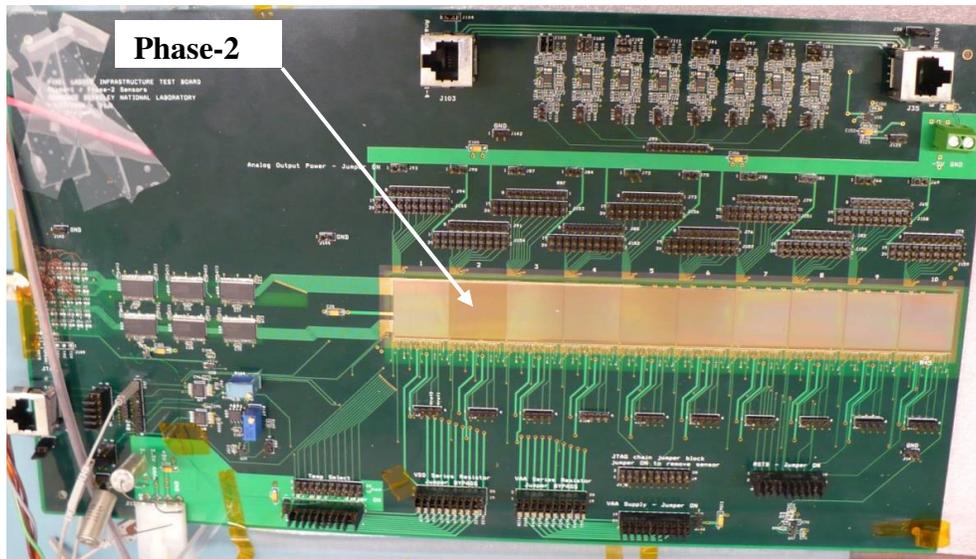


Figure 1 Photograph of the Infrastructure Testing Board (ITB) with 10, full thickness sensor: 9 Phase-1 prototypes and one Phase-2 prototype (indicated with a white arrow).

The ITB has been tested in several different configurations to evaluate sensor performance as a function of:

- power supply voltage
- number of high-frequency decoupling capacitors

[1] http://rnc.lbl.gov/hft/hardware/docs/Phase1/Development_PXL_flex_cable.doc

- power supply distribution scheme

Test setup

The ITB is readout using the prototype PXL readout system based on the Virtex5 evaluation board. ITB and Mass Termination Board (MTB) are connected via 2 m of fine, twisted-pair wires, while MTB and the RDO board are connected via 6-m of a twisted pair cable. This is the configuration of the baseline readout design. The main readout interface used in this series of tests was USB2.

The following main configurations were tested:

1. @ 3.3 V
 - Reference conditions
2. @ 3.0 V
 - Reference conditions for the expected sensors operation at 3.0 V
3. @ 3.0 V + 5 Ohm power resistance
 - Additional resistance between the ITB power supply and each of the sensors
4. @ 3.0 V + C34_35
 - capacitors C34, C35 and their equivalents for all sensors were removed from ITB, effectively reducing the number of VDA and VDD bypassing capacitors by half.
5. @ 3.0 V + C32-35
 - no VDA VDD capacitors (capacitors C32, C33, C34, C35, and their equivalents for all sensors were removed)
6. @ 3.0 V + 0.5C VCLP
 - reduced number of VCLP capacitors (removed capacitors from VCLP at sensors 2, 4, 6, 8, 10)
7. @ 3.0 V + 0C VCLP
 - all VCLP capacitors removed
8. 3.0 V + BUS
 - bus-type power distribution; 2 buses: VDA, VDD

The capacitor removal in these tests was progressive and the test setup labels used throughout this document indicate the most recent changes in the ITB configuration.

The chips were tested using digital and analog readout in all of these configurations. In each case, a full threshold scan was performed on all sensors. The initial characterization of all sensors using analog readout showed that the measurements were consistent. We chose four chips (0, 4, 8) as a representative sample for a detailed analog characterization in all test configurations.

Interaction between sensors assembled in the ladder configuration was studied with low and high levels of activity on the ladder. The former configuration included all sensors' thresholds set high, at 250 DAC, leading to practically no activity on the sensor outputs. In the latter configuration, each sensor was configured for zero threshold to provide maximum switching on its outputs. These two configurations determine the envelope for the actual sensor operation. A Phase-1-based PXL prototype will operate at <300 hits per sensor, which should correspond to the test configuration with low (near zero) activity.

The sensor threshold settings were estimated to be:

chip	0	1	2	3	4	5	6	7	8	9
VREF2	89	85	85	87	79	79	82	81	81	82
VREF1=VREF2	86	130	128	114	129	113	130	91	98	150

The temperature of the setup was controlled using a liquid cooling system with a copper backplate attached to the ITB PCB for conductive cooling. The backplate stretched from sensor 2 to the middle of sensor 9. The room temperature throughout the tests was close to 22 °C and the coolant temperature was 15 °C. The resulting average temperature profile on ITB measured with a touchless thermometer is shown in Figure 2.

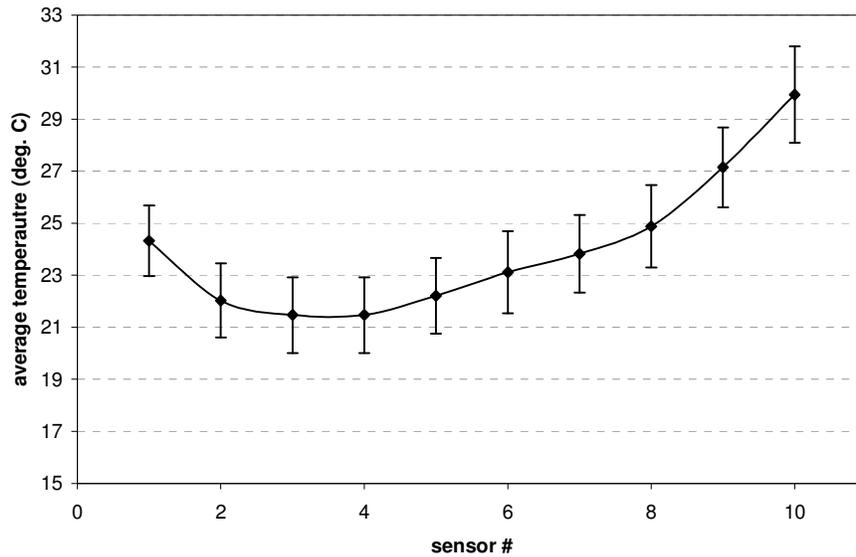


Figure 2 The average ITB temperature profile observed consistently throughout the test.

Noise measurements

We characterize the Phase-1 discriminators in the digital readout mode by performing a threshold voltage scan with the pixel signals connected to discriminators and the sensor located in a dark box. The scan starts with low threshold values that allow all pixels to cross the threshold and be registered as “1” on digital outputs. The scan ends when the threshold is high and no pixel signals pass it. At each scan point we acquire 10 frames of data. This gives us 6400 samples for each discriminator.

To extract the characteristics of each discriminator, we fit the transfer function curve with the complementary error function. The mean value and standard deviation of the underlying Gaussian distribution represent the crossing point and temporal noise, respectively.

The threshold offset dispersion or fixed pattern noise, FPN, in the sensor is extracted as the RMS value of the distribution of crossing points of all 640 discriminators.

The temporal noise of the sensor is extracted as the mean value of the distribution of temporal noise values for 640 columns/discriminators.

Threshold scan results

The test results presented in this section use the following labels:

- 3.0 V – reference run,
- 5_Ohm – test with additional resistance between ITB power supply and each chip,
- C34_35 – half of the power supply decoupling capacitors removed,
- C32-25 – all power supply decoupling capacitors removed
- 0.5xC – half of the original number of VCLP decoupling capacitors,
- 0xC – no VCLP decoupling capacitors,
- BUS – bus configuration with 2 separate VDA and VDD buses,
- REV – is the same BUS configuration, but power is distributed starting from the last sensor,
- 1PWR – the two buses, VDA and VDD, are connected together and only one common power supply is delivered to the ITB.

Figure 3 shows the average noise and FPN value across different test configurations. The noise performance appears to be very stable throughout the test, except for the different bus configurations.

Converting the ITB to a bus structure resulted in damage to some bond wires. As a result, one chip became non-functional, 4 sensors appear to have lost one of the wires on output 3. The missing sensor outputs might, to some extent, affect the test result presented in Figure 3.

The evolution of FPN presented in Figure 3 indicates a slight increase in the average FPN when first decoupling capacitors are removed. This can be mostly attributed to the FPN change in the first chip. At this point there is no clear explanation for this effect other than some damage to the chip. The FPN curve stays very uniform throughout the tests if the first two chips are not included in the calculated average (Figure 3, series marked with a star).

The same observations can be made looking at each sensor individually. The performance of each sensor as a function of the selected setup configuration is shown in Figure 4 and Figure 5, for low and high switching activity, respectively.

Figure 6 shows the fractional noise and FPN change for each sensor as a function of the test setup configuration. The change presented in the plot is calculated using the reference 3.0 V configuration. The data presented in Figure 6 is for low ladder activity. Similar results are plotted in Figure 7 for the high switching activity.

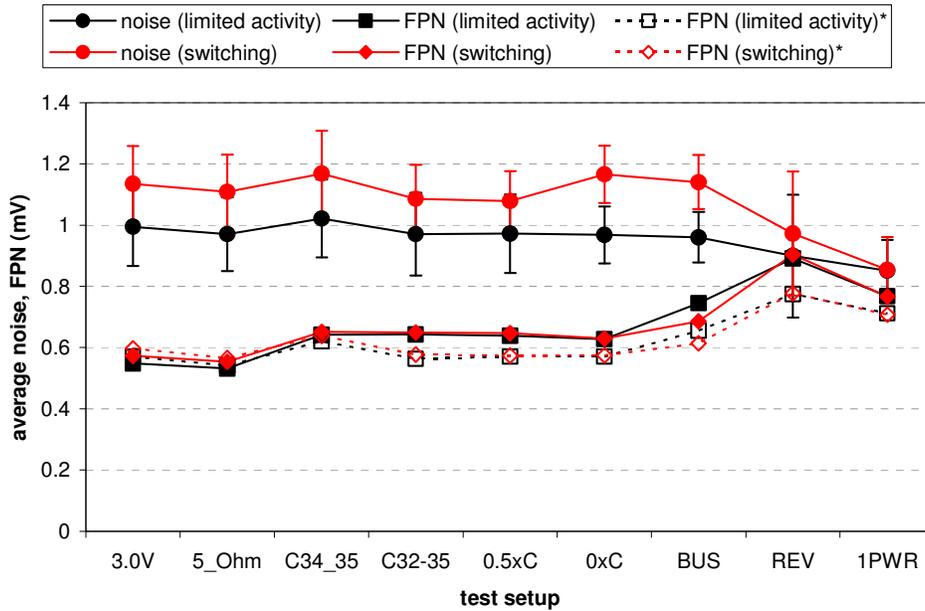


Figure 3 Average noise and FPN extracted from threshold scan measurements for different test setup configurations. FPN data marked with * excludes the first two sensors in the chain. Error bars represent the width (σ) of the noise distribution.

The repeatability of the tests was verified with additional runs. The results are summarized in Table 1. The repeatability is mostly limited to a 4% envelope with averages being most of the time at a 1% level. Some exceptions, which show larger errors up to 34%, are summarized in the last column of the table.

Note that sensor 2 is a Phase-2 prototype, which exhibits a smaller absolute value of FPN

Repeated run	Envelope +/-	average	notes
5 Ohm	4 %	<1%	sensor 10 noise, FPN– 25%
C34_35	4 %	<1%	sensor 2 FPN, noise– 16%
C32-35	4 %	<1%	sensor 2,3 FPN – 25%, 12%
half_C_VCLP	~4 %	<2%	sensor 2 FPN 22%, sensor 4 and 6 noise – 12%, 10%
BUS		<2.5%	sensor 2 FPN 34%, sensor 9 noise 7%

Table 1 repeatability of threshold scans in different ITB configurations.

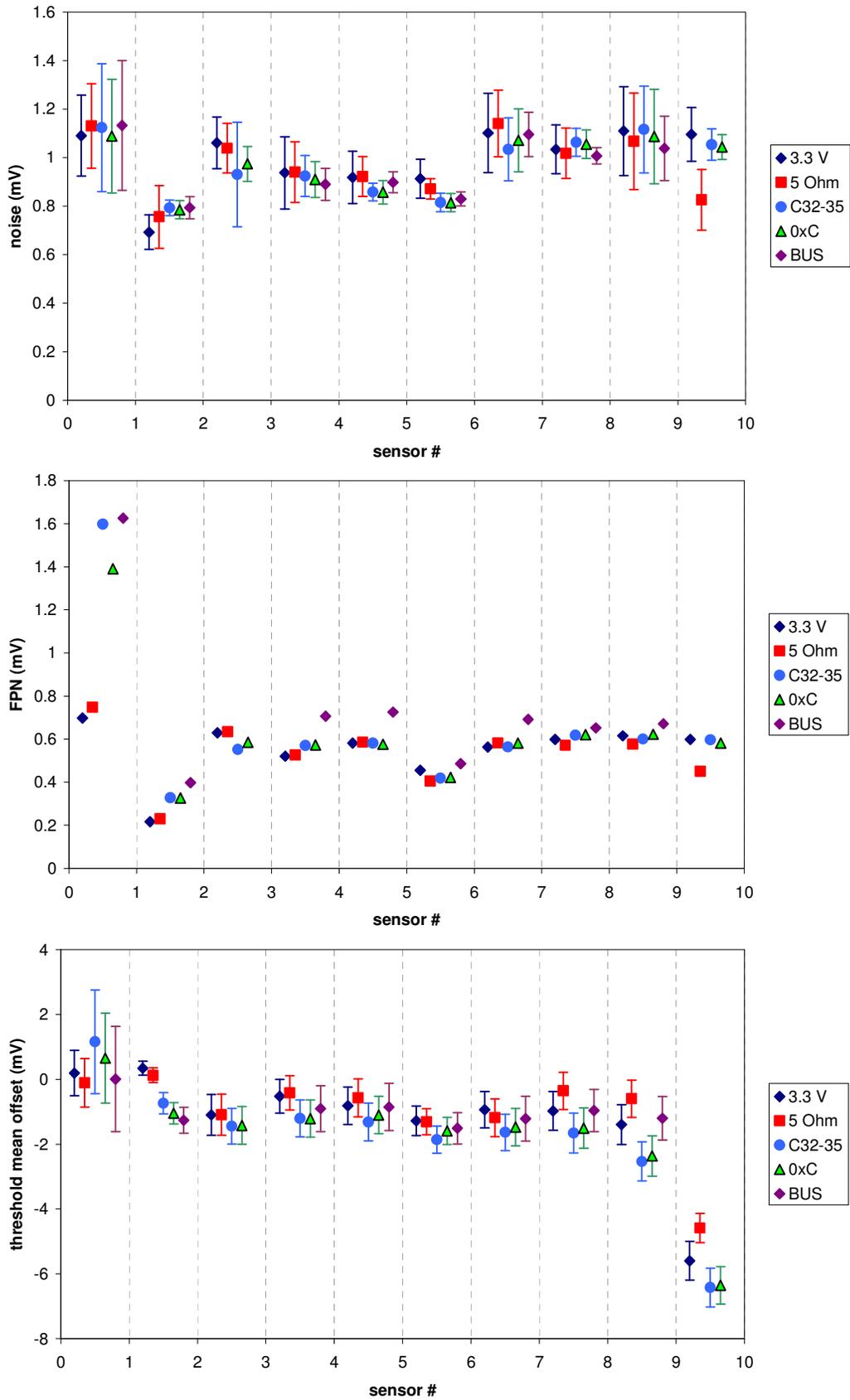


Figure 4 Noise, FPN and threshold mean offset in different test configurations for all 10 sensors tested at low switching activity on the ladder.

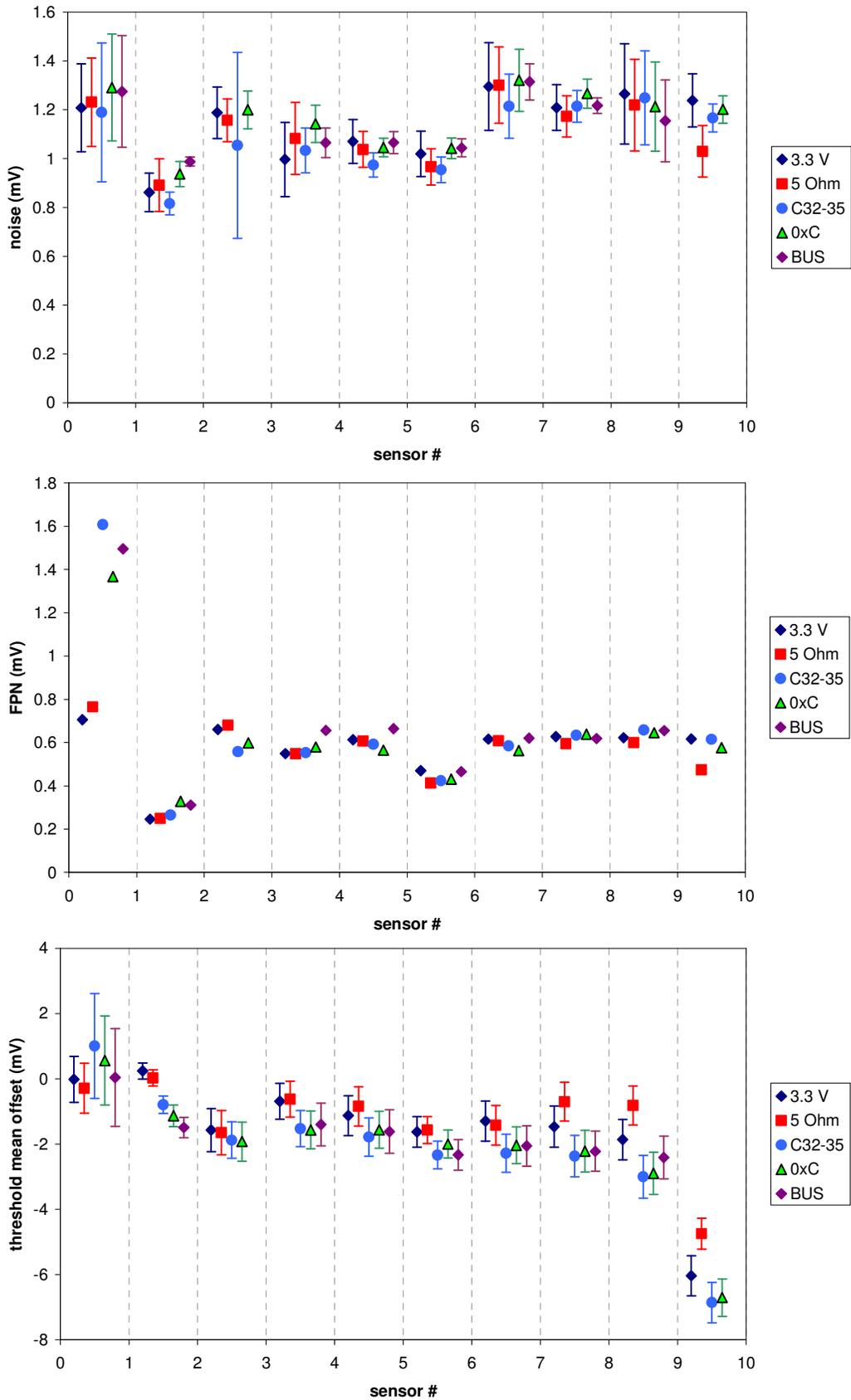


Figure 5 Noise, FPN and threshold mean offset in different test configurations for all 10 sensors tested at high switching activity on the ladder.

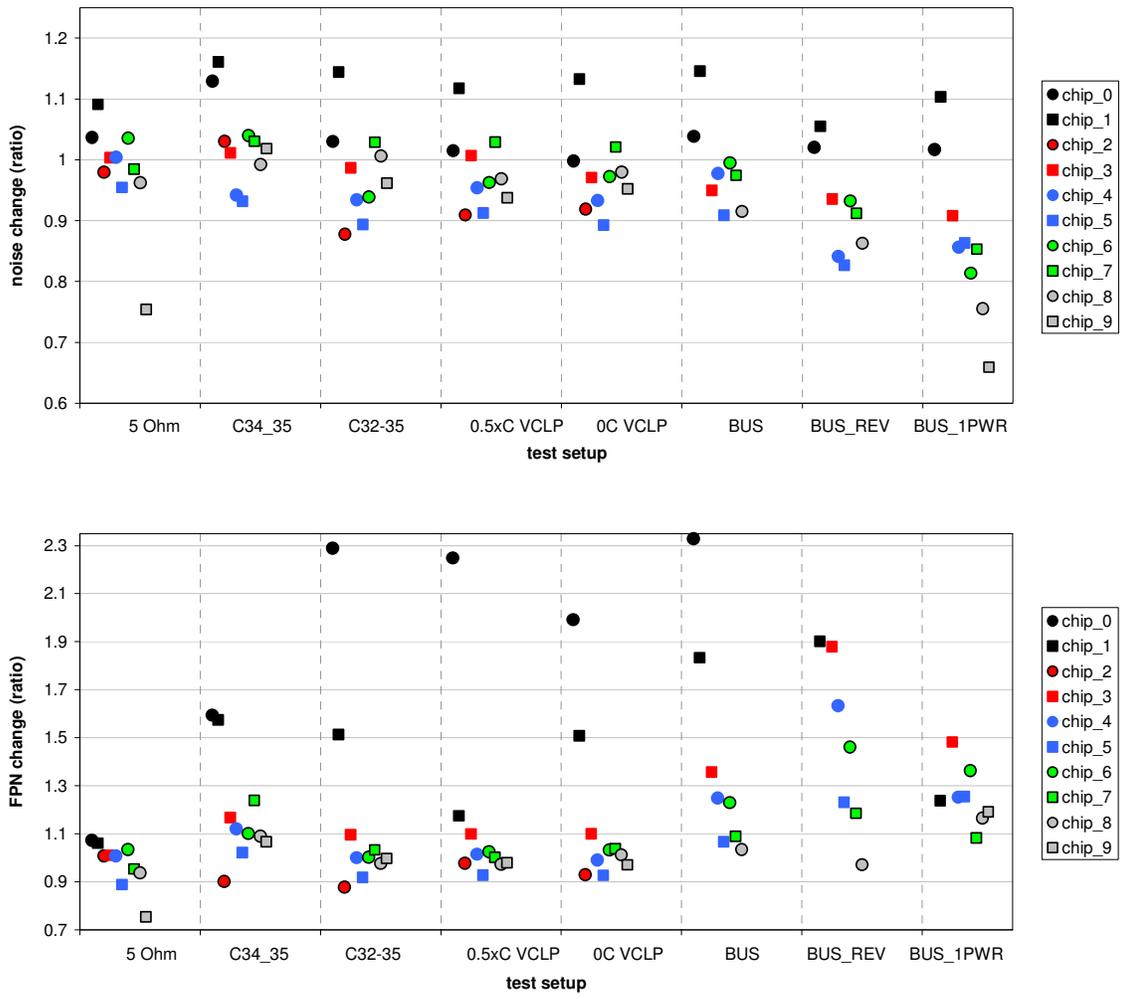


Figure 6 Noise and FPN as a function of setup configuration compared to the default 3.0V operation. Test results for low switching activity conditions.

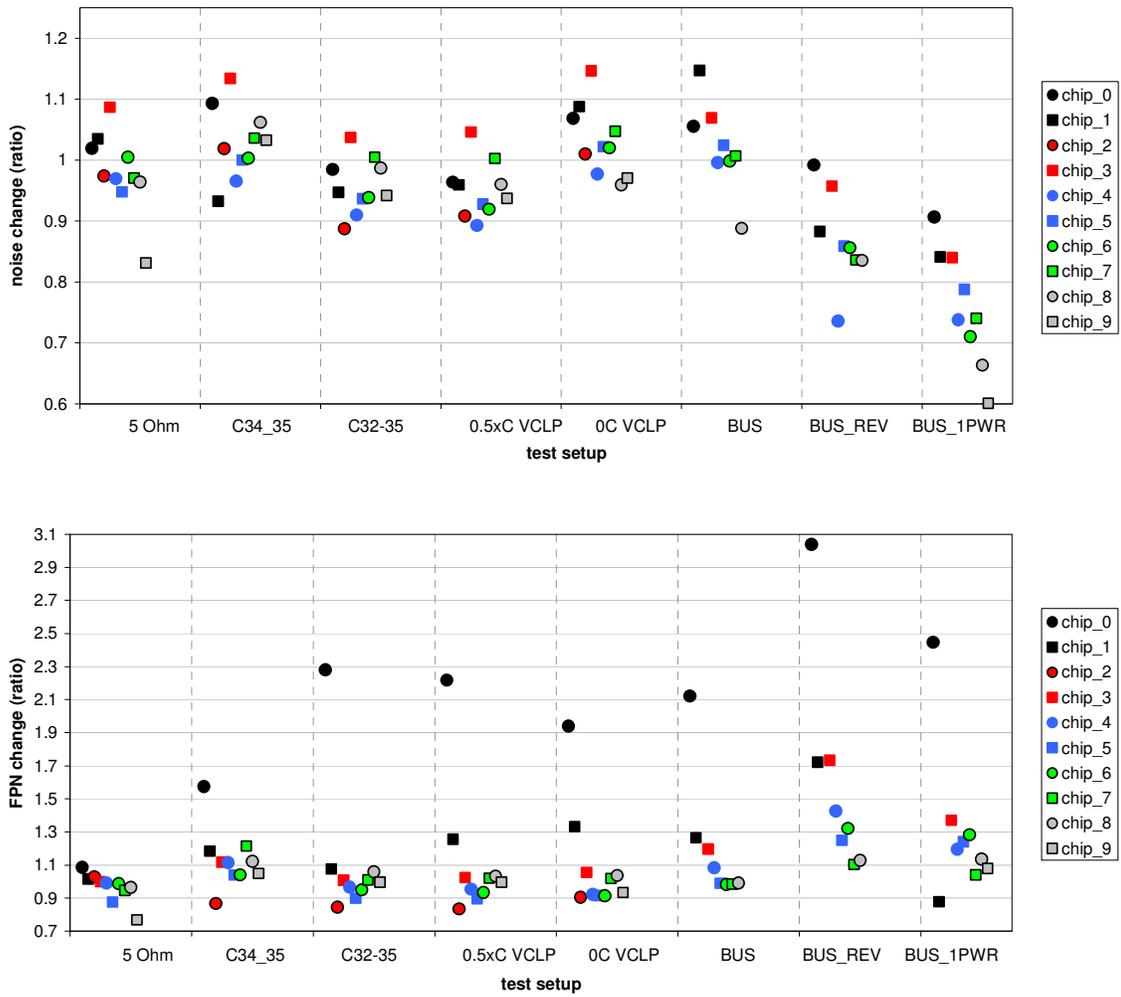


Figure 7 Noise and FPN as a function of setup configuration compared to the default 3.0V operation. Test results for high switching activity conditions.

Analog test results

The test results presented in this section use the following labels:

- Single sensor / ref – each sensor measured individually, other sensors OFF,
- 3.3 V – test at 3.3 V power supply
- 3.0V full others – DUT low activity, other sensors high switching
- 3.0 V* – see above
- 5_Ohm and each chip – test with additional resistance between ITB power supply
- C34,35 – half of the power supply decoupling capacitors removed,
- C32-25 – all power supply decoupling capacitors removed
- 0.5 C – half of the original number of VCLP decoupling capacitors,
- 0.5 C R – as above, repeated measurement
- NO C – no VCLP decoupling capacitors,
- BUS – bus configuration with 2 separate VDA and VDD buses,
- BUS_REV – is the same BUS configuration, but power is distributed starting from the last sensor,

Figure 8 summarizes the overall ladder performance at different activity levels on the ladder. The results show the Equivalent Noise Charge, noise and pedestal measured for all tested sensors.

The three main observations are:

1. The performance is uniform between different sensors and clearly depends on the amount of switching activity on the ladder. It is noticeable in the noise plots that the noise increases slightly as a function of the sensor location. The effect is at the level of 10% across the ladder.
2. Lower voltage (3.0V) improves noise performance,
3. Degradation of noise performance in high switching conditions results from the signal coupling on the ITB and not the internal digital-to-analog coupling in the chip.

Figure 9 shows the evolution of the average ENC, noise and pedestal as a function of different ITB configurations. The performance is very uniform for all tested configurations. The slight degradation of performance in the configuration with a bus-type power distribution could result from the faulty LVDS lines on the damaged sensor outputs (output 3).

Figure 10 and Figure 11 summarize the performance variation compared to the reference test conditions at 3.0 V with low and high switching, respectively. The parameter variation as a function of the test setup is miniscule.

Due to the operator error, the analog output of chip 0 became immeasurable in the middle of the test, and was replaced with chip 1 to maintain 3 representative samples.

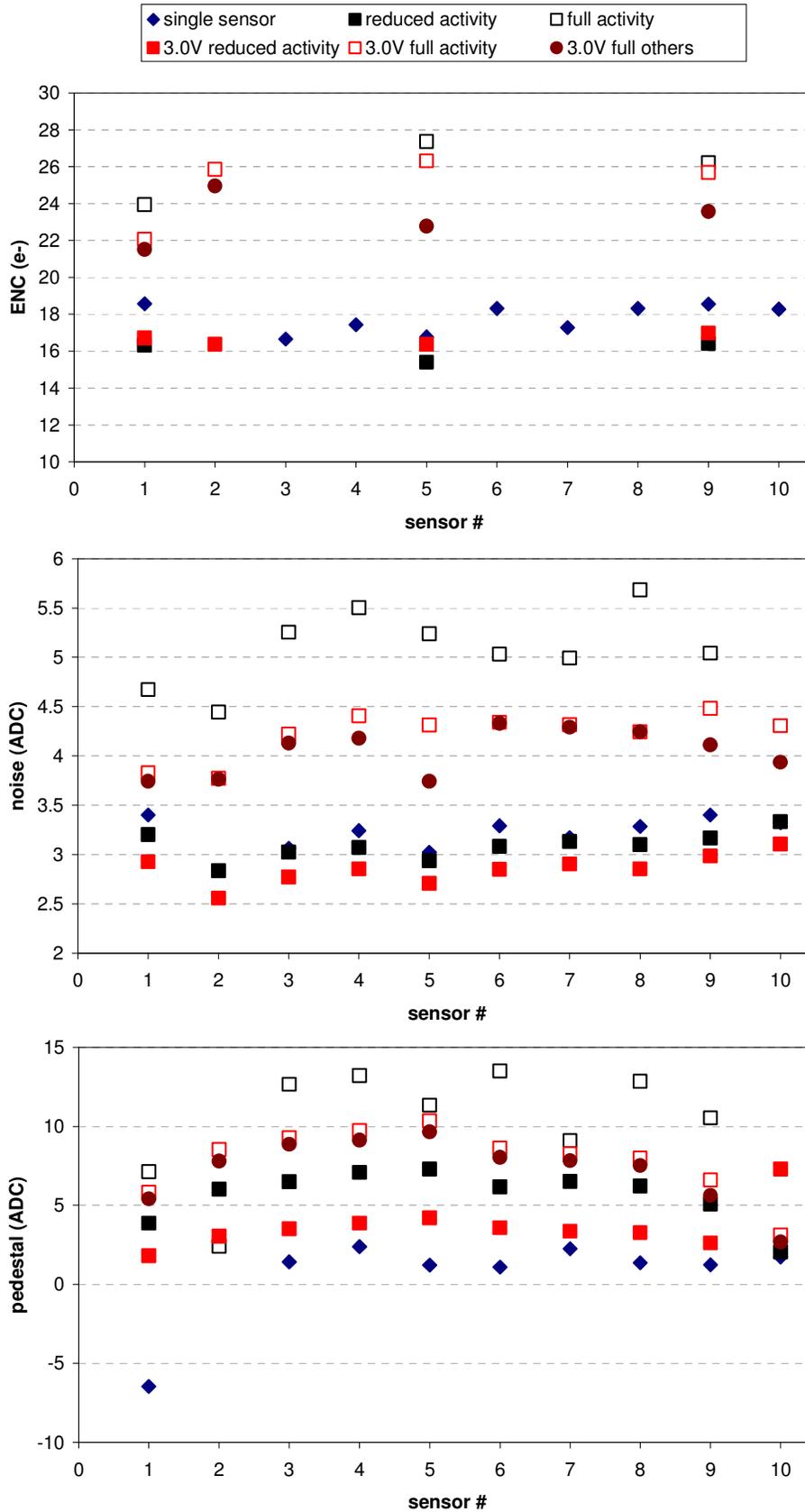


Figure 8 Equivalent Noise Charge, noise and pedestal measured for each sensor running individually and all sensors operating at low and high switching activity levels. “Full others” indicates low activity on the sensor under test and high switching in other sensors.

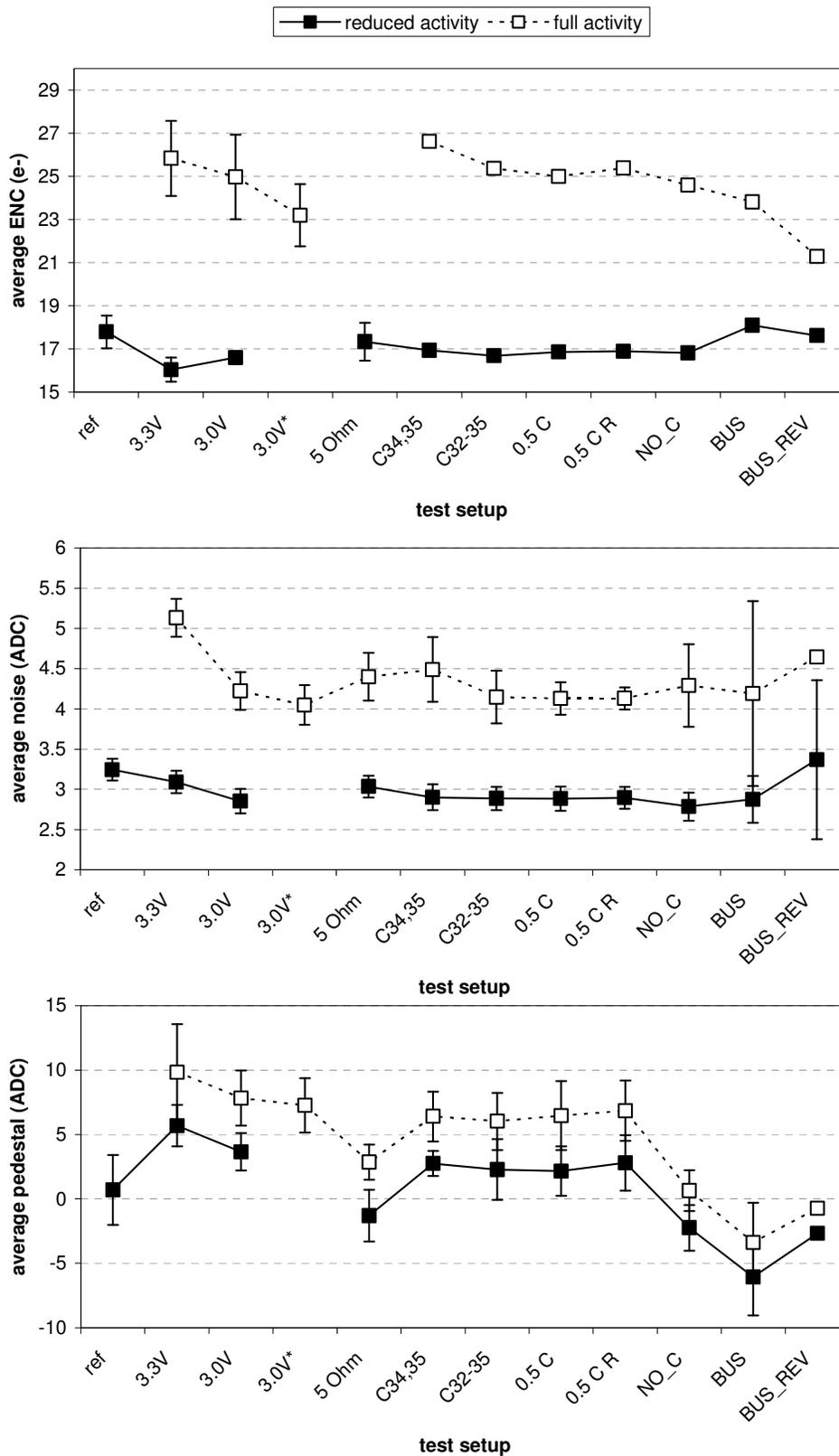


Figure 9 Average ENC, noise and pedestal measured at low and high switching activity levels for different ITB configurations.

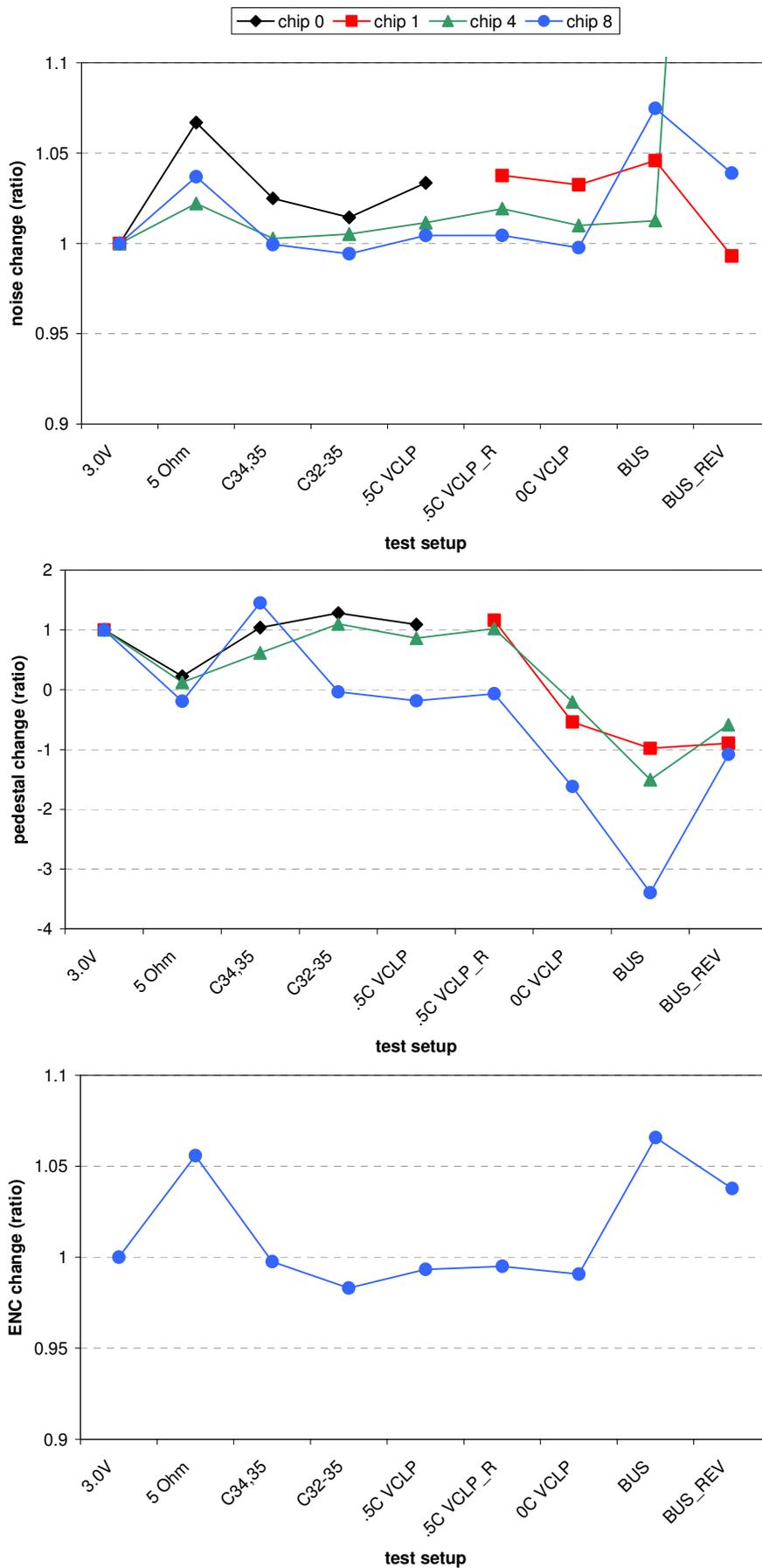


Figure 10 Noise, pedestal and ENC as a function of the ITB configuration compared to the default 3.0V operation. Test results were obtained at low switching activity.

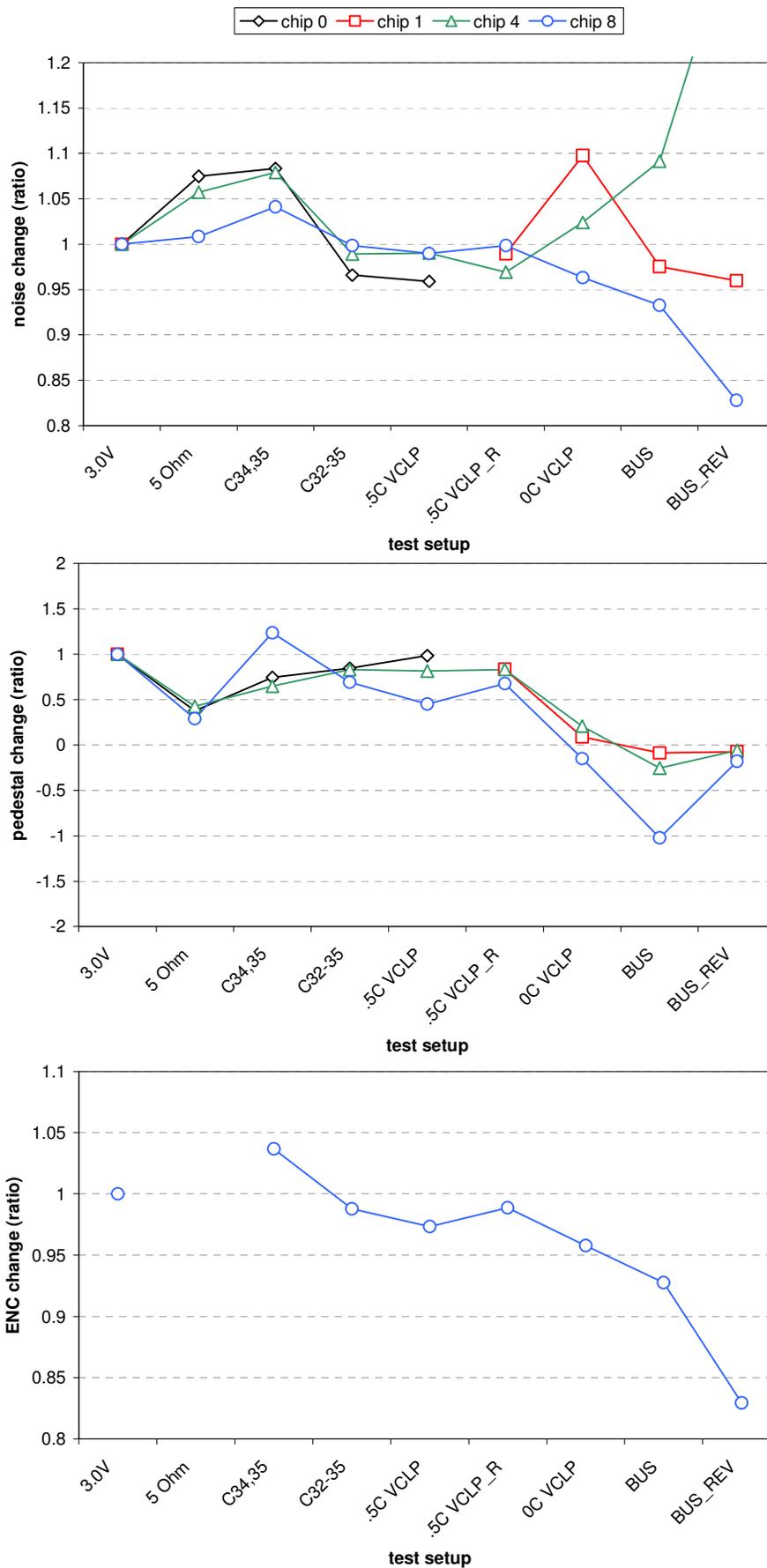


Figure 11 Noise, pedestal and ENC as a function of the ITB configuration compared to the default 3.0V operation. The measurements were performed at high switching activity.

Notable observations:

1. When 5 Ohm resistors were added, it became difficult to obtain a clear calibration peak. The calibration procedure failed completely on chip 0, and failed in one of 4 trials with chip 8.
2. A repeated set of measurements in the “half_C_VCLP” configuration included all sensors. This provides an estimate on the measurement repeatability and a good comparison to results shown in Figure 8.
 - a. Repeatability of measurements confirmed to better than 3% (noise value) [pedestals vary significantly, up to x2 for the last three sensors]
 - b. 17% increase in noise performance across the ladder (Figure 12). However, the maximum noise value is still below the noise level measured at 3.3 V.

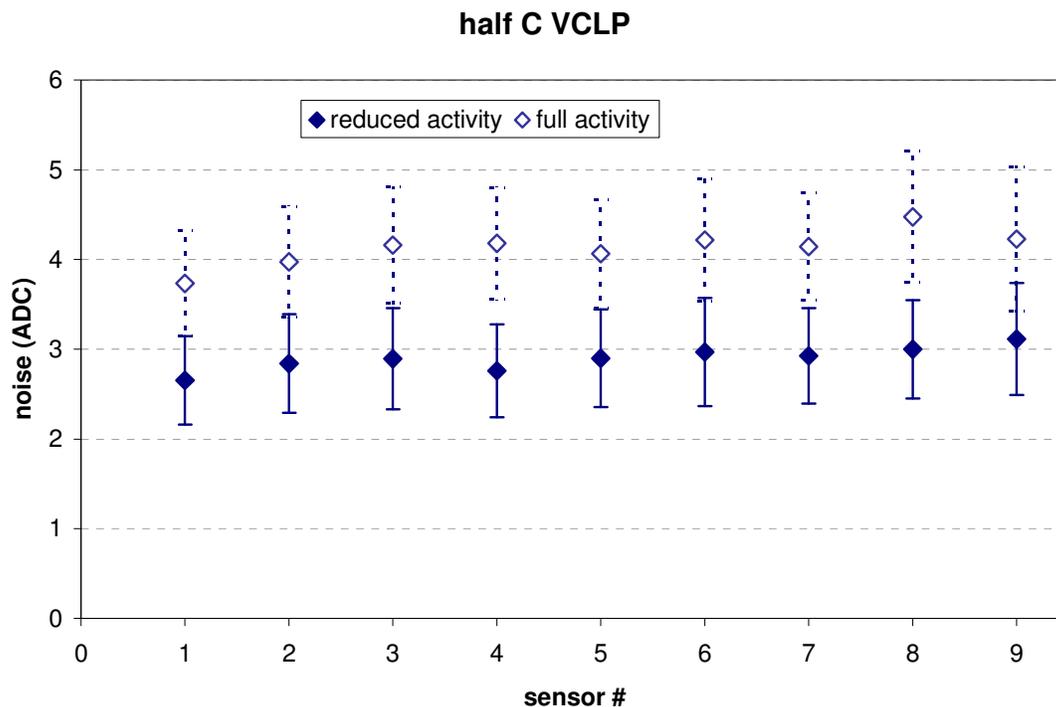


Figure 12 Noise measured on all 9 sensors in the configuration with half of the decoupling capacitance on the VCLP reference voltage.

Summary

Test results obtained with the ITB prototype indicate that the performance of Phase-1 sensors is independent of the ITB configuration, especially the number of high-frequency decoupling capacitors on the board. Both, analog and digital readout modes confirm this observation. The performance is not degraded even after removing all small capacitors associated with VDD, VDA and VCLP voltages.

Test results obtained from threshold scans suggest that the bus-type power distribution provides, on average, a slightly better noise performance but with an increased FPN. Both effects are within 10-20 % and with the damaged sensor readout and limited testing capabilities can not be considered accurate.

Analog test results for the bus-type power distribution indicate that there is no noticeable degradation of the sensor performance. However, the statistics are very limited and significant chip-to-chip variations can be observed.